Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A memory device for driving a display panel comprising:

arrays of memory cells storing binary information;

pairs of bit line-bit bar line connected to the memory cells;

first transfer gates connected to one end of the bit line-bit bar line pairs and switched to access the memory cells;

second transfer gates connected to the other end of bit line-bit bar line pairs and switched to read out the binary information stored in the memory cells; and

data buffers to store the read-out binary information,

wherein signals switching the second transfer gates are derived from a single enable signal and divided into several groups, and the signal for each group has a different time delay.

2. (Original) A memory device for driving a display panel comprising:

a memory cell array storing binary information;

pairs of bit line-bit bar line connected to the memory cells;

first transfer gates connected to one end of the bit line-bit bar line pairs and switched to access the memory cells;

second transfer gates connected to the other end of bit line-bit bar line pairs and switched to read out the binary information stored in the memory cells; and

data buffers to store the read-out binary information,

wherein signals enabling the data buffers are derived from a single enable signal and divided into several groups, and the signal for each group has a different time delay.

3. (Original) A memory device for driving a display panel comprising:

a memory cell array storing binary information;

pairs of bit line-bit bar line connected to the memory cells;

first transfer gates connected to one end of the bit line-bit bar line pairs and switched to access the memory cells;

second transfer gates connected to the other end of bit line-bit bar line pairs and switched to read out the binary information stored in the memory cells; and

data buffers to store the read-out binary information,

wherein signals enabling the data buffers and signals switching the second transfer gates are derived from a single enable signal and divided into several groups, and the signal for each group has a different time delay.

4. (Currently amended) The memory device of ~~any of claims 1 through 3~~ claim 1, wherein the different time delay is performed by a circuit including a logic circuit having an inversing function.

5. (Currently amended) The memory device of ~~any of claims 1 through 3~~ claim 1, wherein the different time delay is performed by a capacitor, a resistor, or a combination of the capacitor and the resistor.

6. (Currently amended) The memory device of ~~any of claims 1 through 3~~ claim 1, wherein the first transfer gates are switched by the column address as being grouped by unit of 2^n , wherein n is a positive integer including 0.

7. (Currently amended) The memory device of ~~any of claims 1 through 3~~ claim 1, wherein the time delay is a signal generated by a plurality of delay portions which are connected in series.

8. (Original) A method of driving a memory device for driving a display panel, wherein data is written on a memory cell array through first transfer gates which are connected to one end of bit lines and partially selected and switched by a column address,

the written data is transferred to data buffers by a switching operation of second

transfer gates connected to the other end of the bit lines, and

the switching operation of the second transfer gates are performed by a signal divided into groups and having a different time delay.

9. (Original) A method of driving a memory device for driving a display panel, wherein data is written on a memory cell array through first transfer gates which are connected to one end of bit lines and partially selected and switched by a column address,

the written data is transferred to data buffers by a switching operation of second transfer gates connected to the other end of the bit lines, and

signals instructing to store the transferred data in the data buffers are divided into groups and have different time delays.

10. (Original) A method of driving a memory device for driving a display panel, wherein data is written on a memory cell array through first transfer gates which are connected to one end of bit lines and partially selected and switched by a column address,

the written data is transferred to data buffers by a switching operation of second transfer gates connected to the other end of the bit lines, and

the second transfer gates and the data buffers corresponding to the second transfer gates are simultaneously operated by signals divided into groups and having different time delays.

11. (Currently amended) The method of ~~any of claims 8 through 10~~ claim 8, wherein the different time delay is performed by a circuit including a logic circuit having an inversing function.

12. (Currently amended) The method of ~~any of claims 8 through 10~~ claim 8, wherein the different time delay is performed by a capacitor, a resistor, or a combination of the capacitor and the resistor.

13. (Currently amended) The method of ~~any of claims 8 through 10~~ claim 8, wherein the first transfer gates are switched by the column address as being grouped by unit of 2^n,

wherein n is a positive integer including 0.

14. (Currently amended) The method of ~~any of claims 8 through 10~~ claim 8, wherein the time delay is a signal generated by a plurality of delay portions which are connected in series.

15. (New) The memory device of claim 2, wherein the different time delay is performed by a circuit including a logic circuit having an inversing function.

16. (New) The memory device of claim 3, wherein the different time delay is performed by a circuit including a logic circuit having an inversing function.

17. (New) The memory device of claim 2, wherein the different time delay is performed by a capacitor, a resistor, or a combination of the capacitor and the resistor.

18. (New) The memory device of claim 3, wherein the different time delay is performed by a capacitor, a resistor, or a combination of the capacitor and the resistor.

19. (New) The memory device of claim 2, wherein the first transfer gates are switched by the column address as being grouped by unit of 2^n, wherein n is a positive integer including 0.

20. (New) The memory device of claim 3, wherein the first transfer gates are switched by the column address as being grouped by unit of 2^n, wherein n is a positive integer including 0.

21. (New) The memory device of claim 2, wherein the time delay is a signal generated by a plurality of delay portions which are connected in series.

22. (New) The memory device of claim 3, wherein the time delay is a signal generated by a plurality of delay portions which are connected in series.

23. (New) The method of claim 9, wherein the different time delay is performed by a circuit including a logic circuit having an inversing function.

24. (New) The method of claim 10, wherein the different time delay is performed by a circuit including a logic circuit having an inversing function.

25. (New) The method of claim 9, wherein the different time delay is performed by a capacitor, a resistor, or a combination of the capacitor and the resistor.

26. (New) The method of claim 10, wherein the different time delay is performed by a capacitor, a resistor, or a combination of the capacitor and the resistor.

27. (New) The method of claim 9, wherein the first transfer gates are switched by the column address as being grouped by unit of 2^n, wherein n is a positive integer including 0.

28. (New) The method of claim 10, wherein the first transfer gates are switched by the column address as being grouped by unit of 2^n, wherein n is a positive integer including 0.

29. (New) The method of claim 9, wherein the time delay is a signal generated by a plurality of delay portions which are connected in series.

30. (New) The method of claim 10, wherein the time delay is a signal generated by a plurality of delay portions which are connected in series.